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Silicon integrated capacitance for power conversion applications

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Outline

- Introduction
- New architecture of capacitive elements (MOSAIC)
  - 3 levels structure
  - **Scalable** capacitor with Low ESL /ESR (tunable)
- Development of physical model
  - Predicting the electrical behavior
- Electrical characteristics in the RF domain (300Khz – 1Ghz)
  - Benefit in term of component parasitics (ESR /ESL) compared to prior art
  - Simulation Vs Measurement
- Example of application: ***PowerSwipe Project***
  - Typical application schemes in the field of the analogic high frequency power conversion
  - Need for better reliability and low profile SiP (ultra-thin capacitors down to 80µm)
- Conclusion and future outlook

Who are we?

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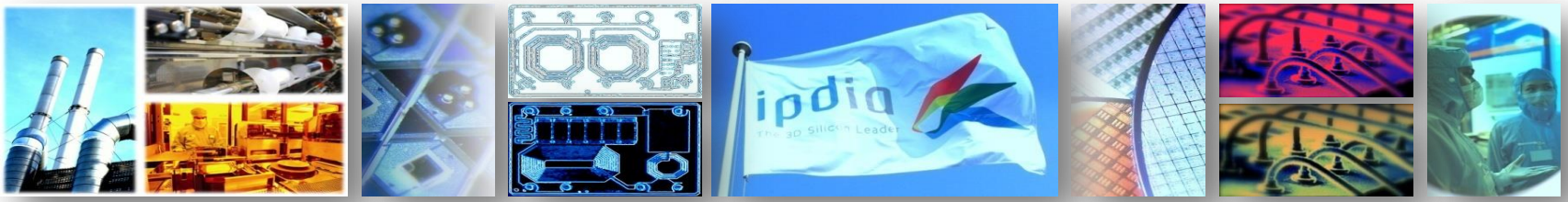
Who are we?

- Independent European High Tech Company
- Dedicated to the manufacture of cutting edge Integrated Passive Devices
- Operate own 10 000 m² (110 000 ft²) Silicon wafer facility
- 20 M$ incomes, 105 people
- 25% of financial resources allocated to R&D
- Technology adopted by 3 of the top 5 leaders in medical electronics as well as by key players in the semiconductor area and HI-Rel industry



IPDiA terminology

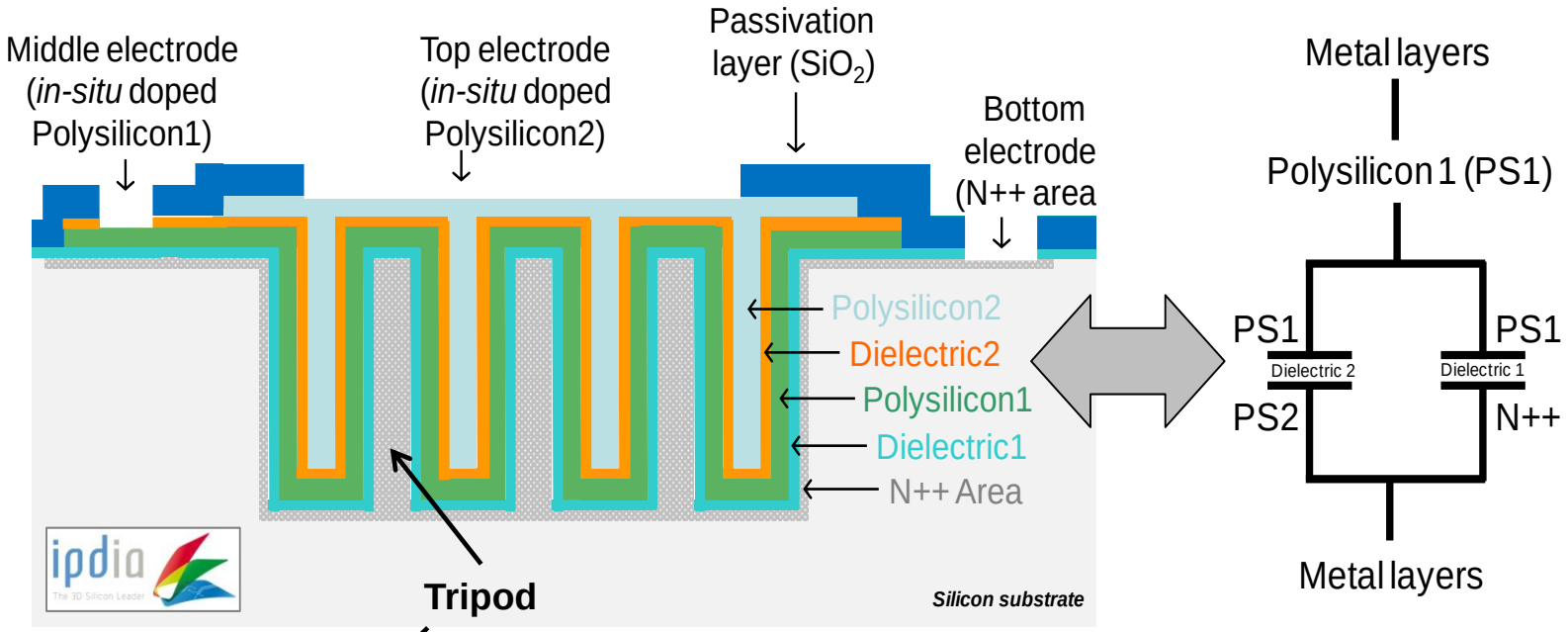
– PICS (Passive Integrated Connective Substrate) technology

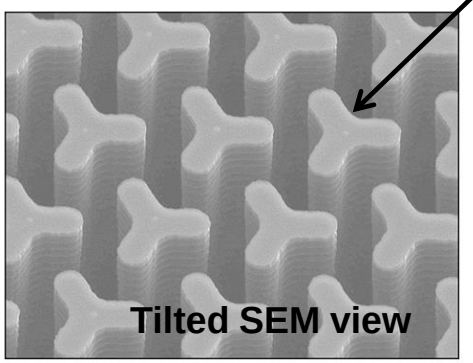
- *3D capacitors (Deep trench Capacitors)*
- *MIM Capacitors*
- *Inductors*
- *Polysilicon Resistors*
- *TSVs*
- *Diodes*

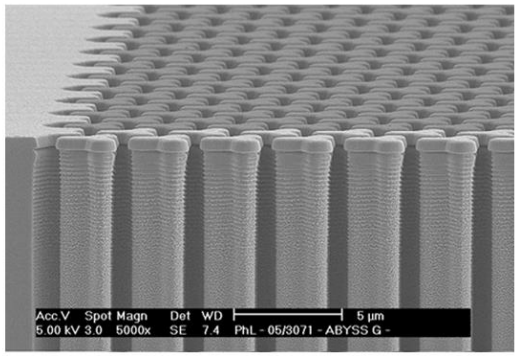
'Functionalized' PICS interposer

3D structure

2 parallelized capacitors in a MIMIM architecture to increase the capacitance value



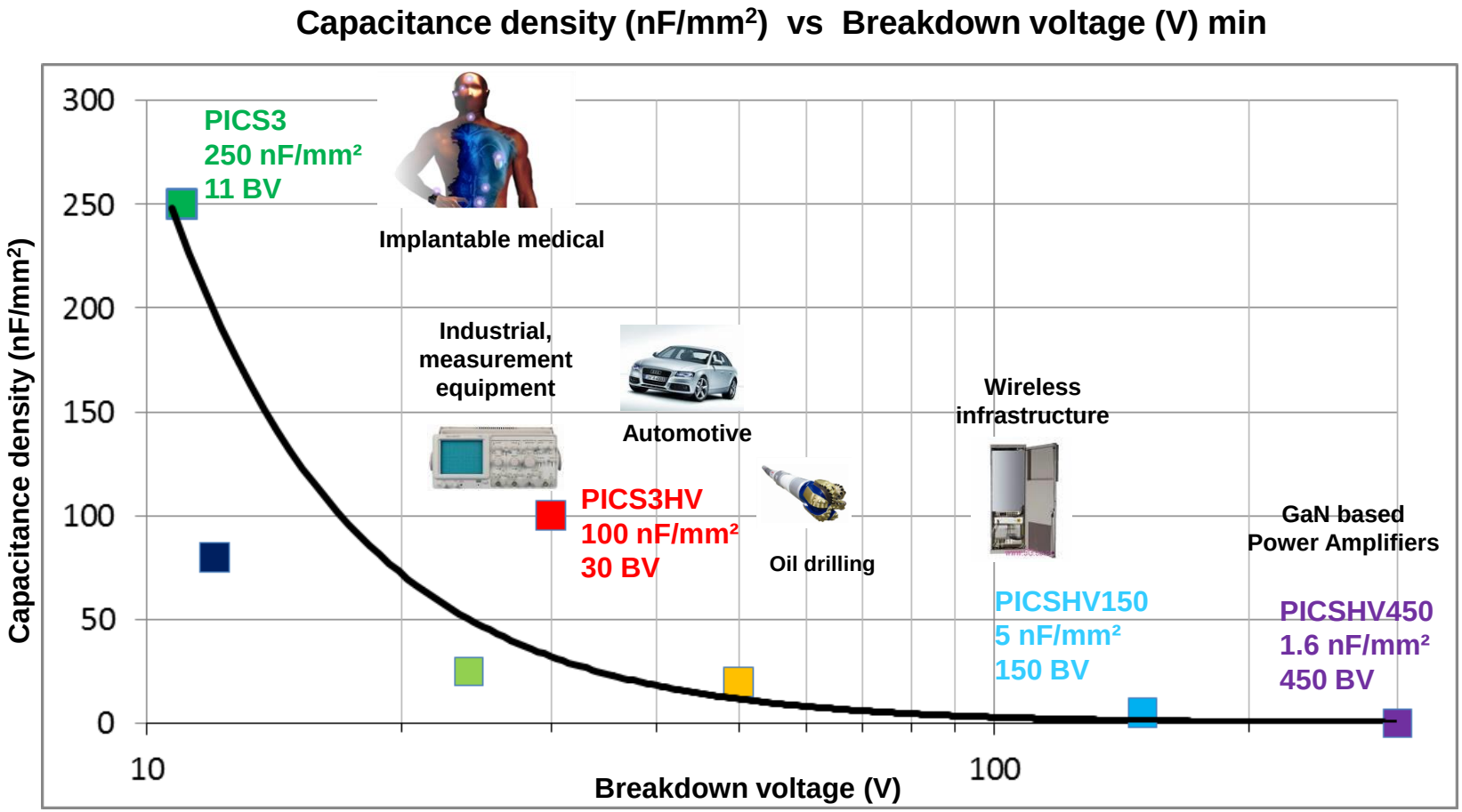




Patents

- US8085524 + other countries
- US8729665 + other countries
- US8283750 + other countries

Diversity of current IPDiA trench process technologies



Capacitors Performances Summary

- Breakdown voltage from 10V to 100V
- Low leakage current <1nA/mm² @ ambiant / Vnom
- Excellent temperature and voltage linearity
  - *< 100ppm/˚K & < 100ppm/V*
  - *Silicon capacitors and arrays are insensitive to operating temperatures between – 65˚C to 250˚C*
- Excellent matching < 2%
- High reliability
  - *> 10 yrs @ operating voltage @ 100˚C*
  - *FIT (Failure in Time) below 1 @ 225˚C*
  - *Mechanical shock tests pass easily as well as thermal cycling tests (up to 3000 cycles in TMCL)*
- Low Profile (ultra-thin capacitors down to 80µm)
- Low ESR/ESL

Electrical characteristic in the RF domain

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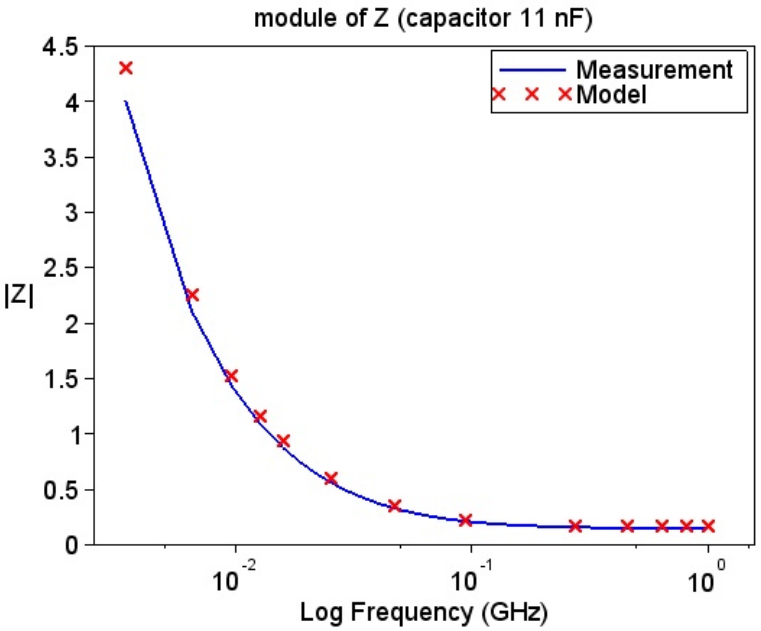
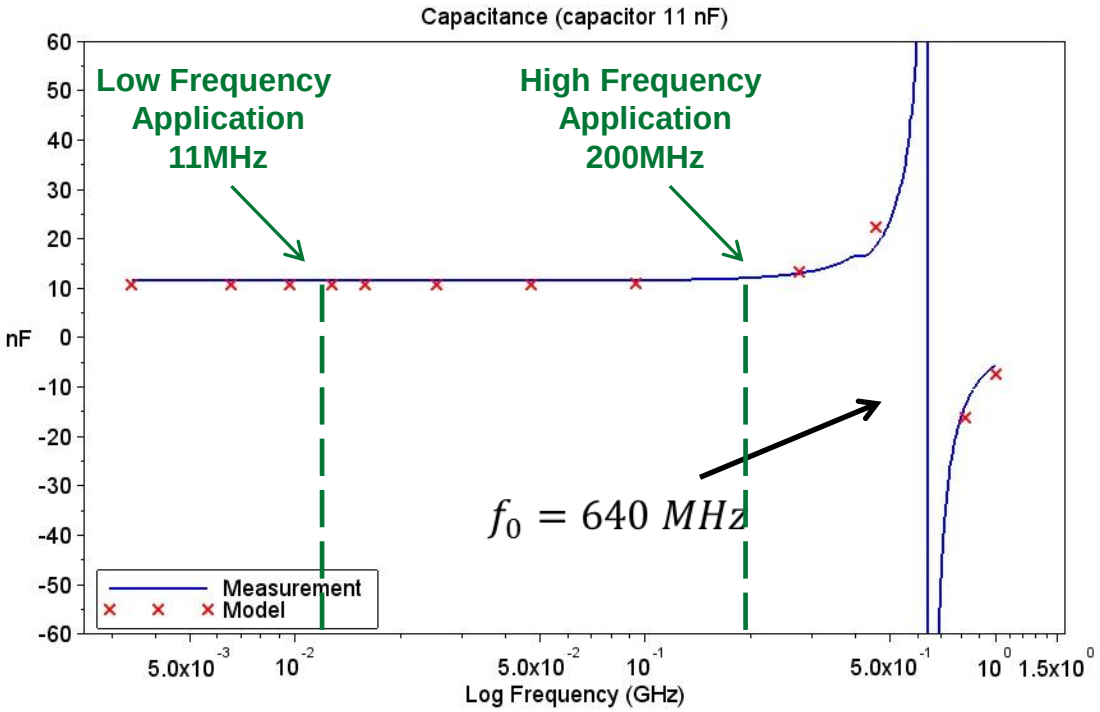
Measurements and model comparison

- **11 nF mosaic capacitor (22 tripods by cell), 10x10 cells, C tripod = 5pF**





- Good matching between model and measurement
- Stable capacitor value up to ~300MHz
- Very high resonance frequency (640 MHz)

Measurements and model comparison

	C (nF)		R (mΩ)		L (pH)		f_0 (MHz)	
	model	measure	model	measure	model	measure	model	measure
11 nF	11.4	11.6	164	156	5.4	5.3	640	643
16 nF	16.3	16.7	113	117	6.1	5.5	505	525
33 nF	33.1	33.5	56	71	5.9	6.7	360	335
222 nF	223.2	224	8	28	4.2	4.1	165	167
470 nF	473	468	4	24	2.9	2.2	136	157
404 nF	390	392	4	40	4.91	1.53	115	205
406 nF	390	391	3	35	5.3	3.31	110	140

Example of application

Power Swipe Project

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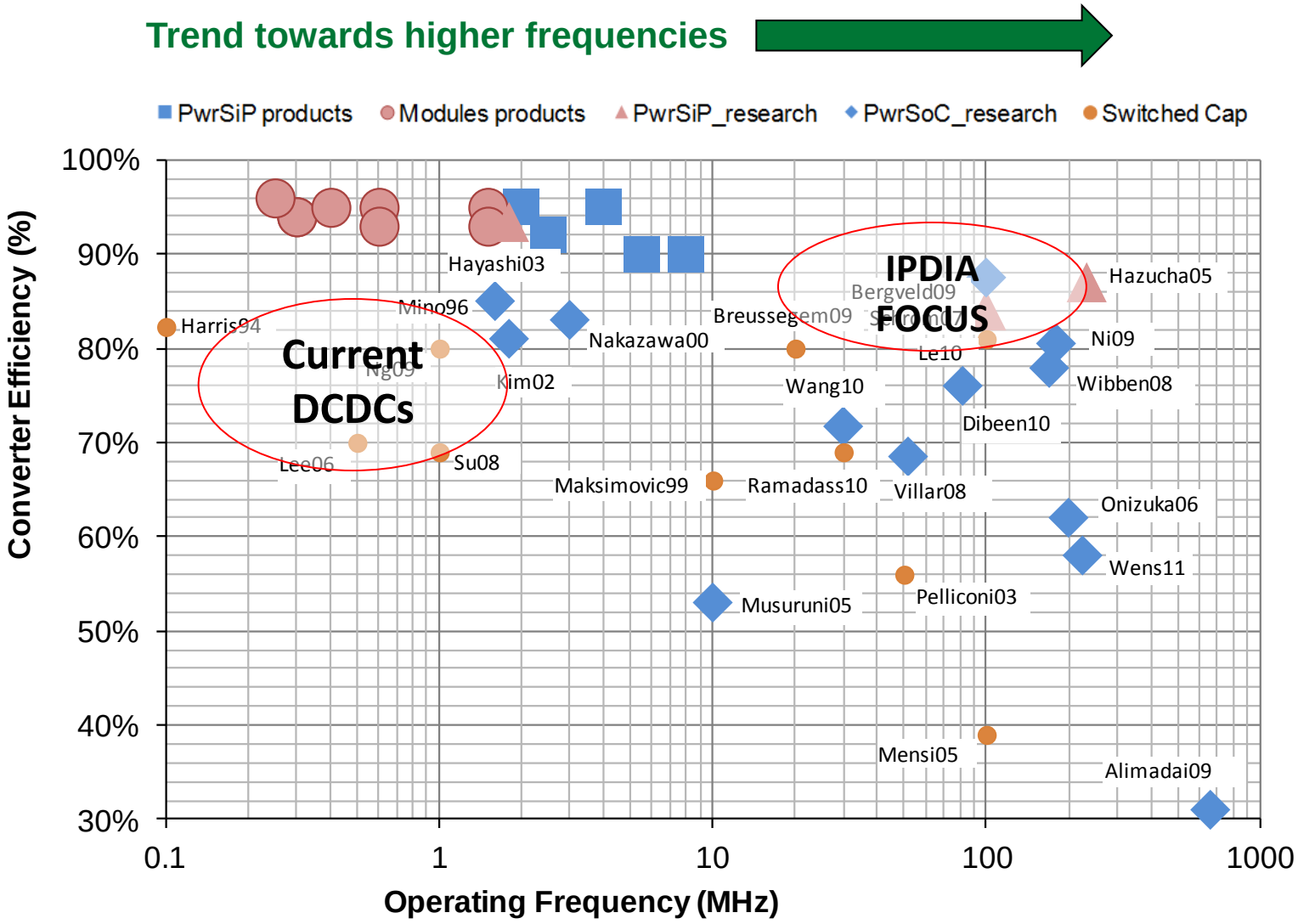
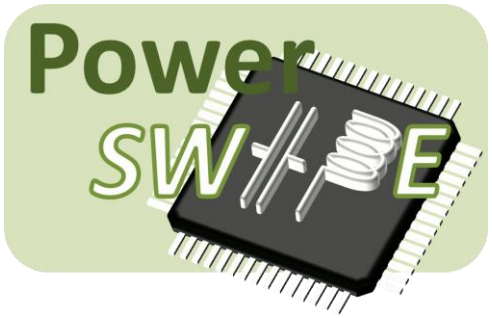
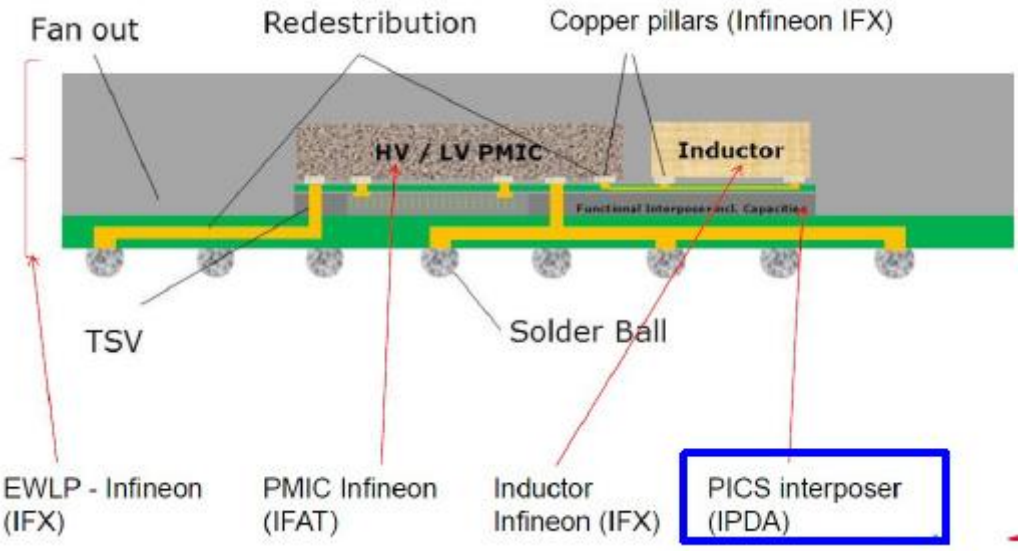
MOSAIC capacitors for power conversion

Trend towards higher frequencies



MOSAIC capacitors for power conversion





- IPDiA Trench capacitor technologies allow potential solution for LC interposer as part of PwrSiP platform

Low Frequency

L = 250nH, C = 400nF, **F=11Mhz**, P=1W.
Cap density: **250nF/mm² Low voltage**
70nF/mm² High voltage
ESR ~ 50mOhm **target <100mOhm**
SFR > 100Mhz
Dual voltage : HV <16V and LV <5V
P ~1W
Efficiency =90%(LV) / 80% (HV)

High Frequency

L = 30nH, C = 30nF, **F=200Mhz**, P=1W.
Cap density: **220nF/mm²**
ESR ~ 50mOhm **target <100mOhm**
SFR > 100Mhz
Vmax=4V (typ 3.2V)
P ~1W
Efficiency =90%

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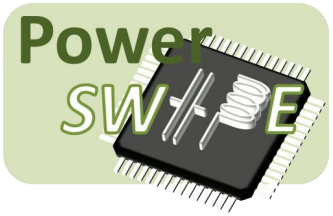
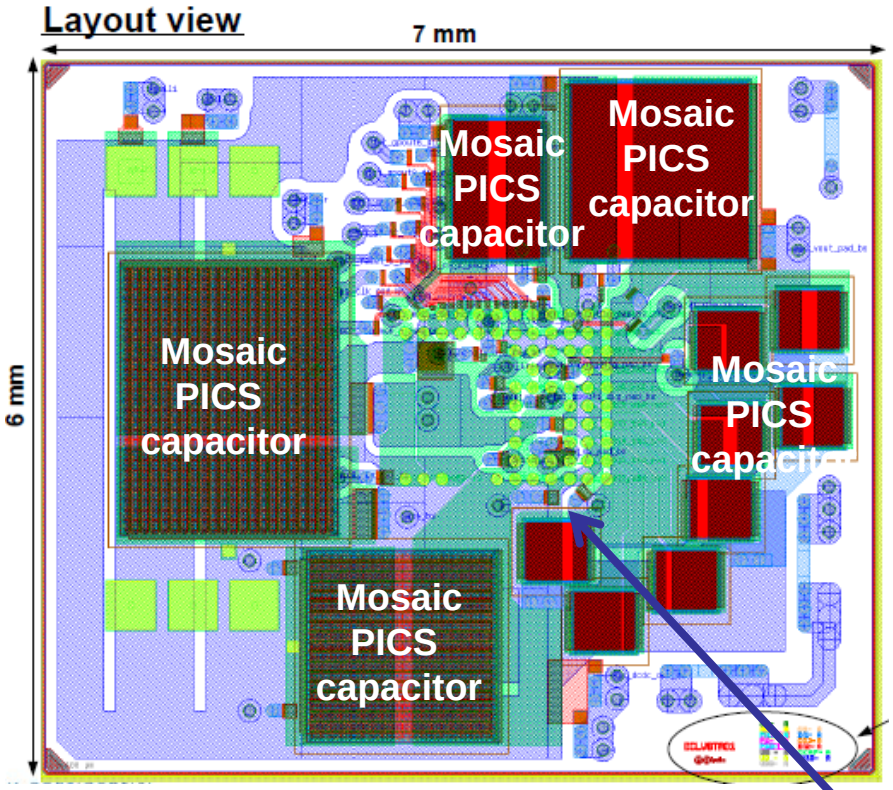
MOSAIC capacitors for power conversion

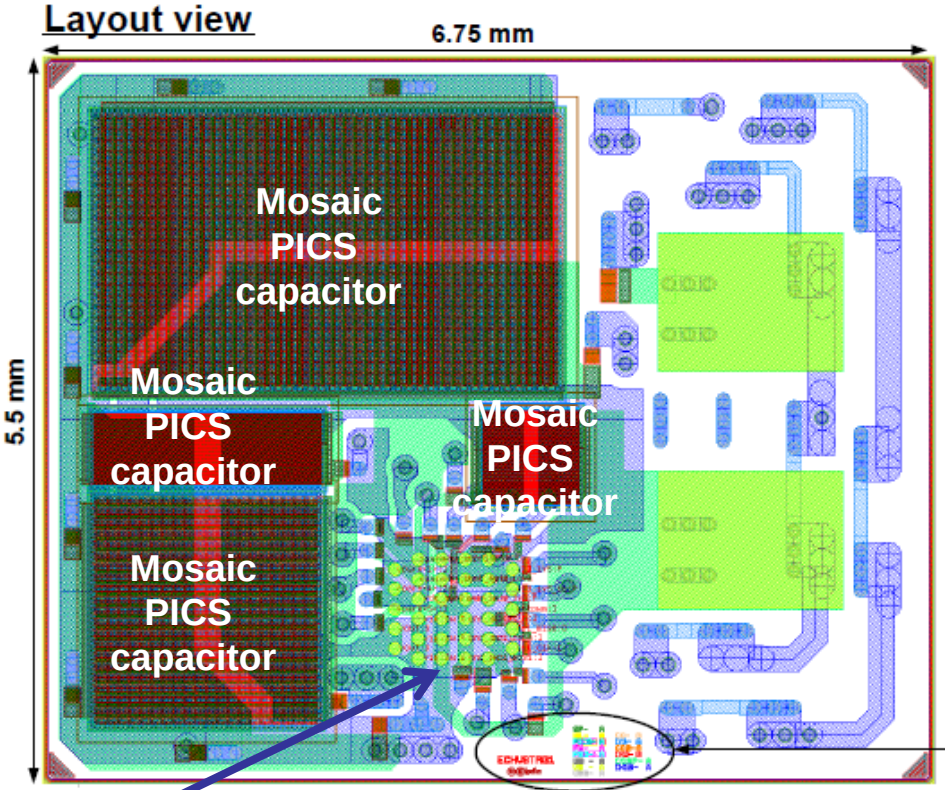


Low voltage



250nF/mm² / 11V

High voltage



70nF/mm² / 35V

Power management integrated circuit

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MOSAIC capacitors for power conversion

- Capacitors benefits:
  - High resonance frequency
  - Low ESR / ESL
  - Low profile, high reliability and stability (T,V)

- Routing benefits:
  - Very compact routing → interposer is 6mm x 7mm
  - Very low inductive traces achievable by leveraging metal levels:
    - 3 top metallization layers (Thick Cu)
    - 1 backside metallization (Thick Cu)
  - Vertical interconnect with TSV

HV interposer:

- RLC extraction on interconnection nets
- ESR estimated for DC
- Inductances extracted @ 11Mhz
- Optimization on critical nets

Critical nodes

name	R (mohm)	L (nH)
	calculated	simulated
vdd_hs-Chs_in	48	0.8
Chs_out-L_in	33	1
vin-C_in	20	0.6
Cin_out-GND	26	
vout-Cout_in	40	
Cout_out-GND	70	5.8
SW-L_in	61.5	1.65
L_out-current prob	61	
gnd_io-gnd_pwr	18	
gnd_pwr-GND	34	
vdd_ls-C_ls_in	90	
C_ls_out-GND	39	
spare<1>	62	
spare<2>	74	
spare<3>	65.5	
spare<4>	58	
spare<5>	58	
spare<6>	226	
extpwm	62	
reset_n	99	
spi_clk	67	
spi_cs_n	71	
spi_mosi	61	
spi_miso	61	
vdd_3v3	74	
vdd_1v5	65	
vdd_1v5_io	65	
vbg_1v2	62	
ibp_test_4u	69	

Conclusion and future outlook

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Conclusion

- IPDiA MOSAIC technology is **C scalable**, integrable in **low profile interposer**

- When C scaled
  - SRF is driven by RLC of the most elementary building block
  - Linear dependency with $C_{global}=N*C_{local}$ where N is the number of repetitions of the localized element
  - **Inverse linear dependency for the ESR and ESL** with $L_{global}=L_{local}/N$ and $ESR_{global}=ESR_{local}/N$ (electrode resistivity is thus becoming secondary)
  - Demonstrated C scaling technique ➔ based upon physical model and measurements

- DC/DC converters: trend towards higher frequency ➔ IPDiA Moasic capacitors are **well suited**.

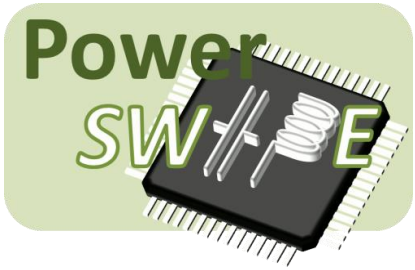
- **Best trade off** between C value, ESR target, ESL target @ interposer level

- **Flexibility** (full-option solutions) can make the difference
  - High Voltage / Low Voltage; Low frequency / High frequency; Isolation requirements → Isolation strategies.
  - Customized Design / Customized Process

Acknowledgments

The authors would like to thank :

- PowerSwipe project partners http://www.powerswipe.eu/



- CarrICool project (IPDiA PICS interposer) → E-Poster Session #6

- *IPDiA team @ PwrSOC 2014 → We have solutions for you*

Thank you for attention !

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